REMARKS

This amendment is being filed as a response to the Office Action of August 19, 2009. Reconsideration is respectfully requested in view of these clarifying amendments and remarks.

Rejections under 35 USC § 103(a)

Claims 1-20 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Narayan et al. (US Patent No. 5,822,559), in view of Kregness et al. (U.S. Patent No. 4,595,911). This rejection is respectfully traversed. Applicants respectfully request reconsideration of these rejections in light of the amendments and arguments contained herein.

Present claims 1, 7, and 14 define an input socket configured to receive data associated with a processing stage of a data packet, each processing stage of the data packet being associated with one network protocol from a plurality of network protocols in the data packet (see this or similar, but not necessarily identical language in claims 1, 7, and 14). In the Response to Arguments, the Examiner has asserted that the "term packet is broad enough to cover any transfer of bits" (page 12, third paragraph). Applicants respectfully disagree, as discussed on pages 4-6 of the Appeal Brief filed April 22, 2009. Nevertheless, in the spirit of expediting the prosecution of the present application, Applicant has amended each of the independent claims to further distinguish Applicant's claim language from the above reference. Present claim 1 defines that the data is associated with a processing stage, and that each processing stage is associated with one network protocol from a plurality of network protocols in the data packet. Neither one of these features is taught by Narayan.

According to the Office, Narayan teaches "data received by a processor" (page 3, last parg.). However, Narayan does not teach an input socket configured to receive data associated with a processing stage of a data packet, each processing stage of the data packet being associated with one network protocol from a plurality of network protocols in the data packet, as claimed by applicants.

Further, present claim 1 defines a network application processor with circuitry configured to access data structures associated with the received data and with the corresponding network protocol. Narayan does not teach a processor that access the data structures associated with the corresponding network protocol. Narayan teaches "Superscalar microprocessors achieve high performance by executing multiple instructions concurrently and by specifying the shortest possible clock cycle consistent with the design" (col. 1, lines 12-15). However, Narayan is silent with respect to a processor that accesses data structures associated with a network protocol.

Further, claims 1 and 7 have been amended to define circuitry enabling single clock cycle access of an operand, as suggested by the Examiner. Additionally, Applicants have clarified that the circuitry [is] configured to access data structures and enabling single clock cycle access of an operand from memory during consecutive clock cycles. The Examiner has asserted that Narayan teaches this feature in Fig. 20 and corresponding text "regarding fetching instructions in one clock cycle" (page 4, first parg). Narayan teaches in Fig. 20 one cycle for fetching, another cycle for scanning, another cycle to multiplex instructions, etc. However, Narayan does not teach accessing an operand in a single clock cycle during consecutive clock cycles, because Narayan teaches different operations in the different

cycles, which means that there are clock cycles between fetches. Thus, there are no fetches of operands during consecutive clock cycles.

Additionally, claim 21 has been added to further define the single clock cycle operation. Claim 21 defines, an instruction fetch and decode operation, and an execute and write back operation, where the execute and write back operation is executed simultaneously with the instruction fetch and decode operation for the next instruction following the execute and write back operation. Narayan teaches different operations in the different cycles, but Narayan does not teach concurrent operations every clock cycle. Thus, Narayan does not teach the specified features in reference to the single clock cycle access.

Furthermore, claim 7 has been amended to further clarify the use of a mask. Claim 7 specifies that the first operand is masked by a mask in the corresponding instruction to enable the ALU to process a non-masked segment of the first operand. Narayan teaches the following:

> "The write-back interface of the FIROB is to ensure the retiring of instructions in program order. In addition to controlling write back to the register file, the FIROB updates the EIP register and flags registers and controls the order of the load-miss, store accesses and move-to-special-register instructions. In normal operation, the FIROB retires an entire line of instructions at a time. All instructions in the line must have the valid results from the functional units or LSSEC. All entries with valid result destination will write back to the register file. The LIL and NC status bits of the FIROB ensures that none of the write-back destinations are the same. The destination address includes the selected bytes for writing back data. In the case LIL and NC status bits are set for destinations of different size, and the FIROB masks the selected bytes before sending to the register file. In some special case, the FIROB retires a partial line. The LIL and NC status bits must be checked and reset before retiring, an extra cycle is needed for this case. The LIL and NC status bits are also used for the flags to simplify updating the flags registers" (col. 144, lines 46-65, emphasis added).

Thus, Narayan teaches that the destination address includes the selected bytes for writing back data. However, Narayan does not teach a mask in the corresponding instruction, as claimed by Applicants.

In view of the foregoing, the Office is requested to withdraw the rejection of claims 1, 7, and 14 under §103. The dependent claims are submitted to be patentable for at least the same reasons that the independent claims are believed to be patentable. The Applicants therefore respectfully request reconsideration and allowance of the pending claims. A Notice of Allowance is respectfully requested.

If the Examiner has any questions concerning the present amendment, the Examiner is kindly requested to contact the undersigned at (408) 774-6920. If any other fees are due in connection with filing this amendment, the Commissioner is also authorized to charge Deposit Account No. 50-0805 (Order No. ADAPP223).

Respectfully submitted,
MARTINE PENILLA & GENCARELLA, LLP

/Jose M. Nunez/

Jose M. Nunez
Reg. No. 59,979

710 Lakeway Drive, Suite 200
Sunnyvale, CA 94085
Telephone: (408) 774-6920
Facsimile: (408) 749-6901
email: jose@mpiplaw.com
Customer Number 25920